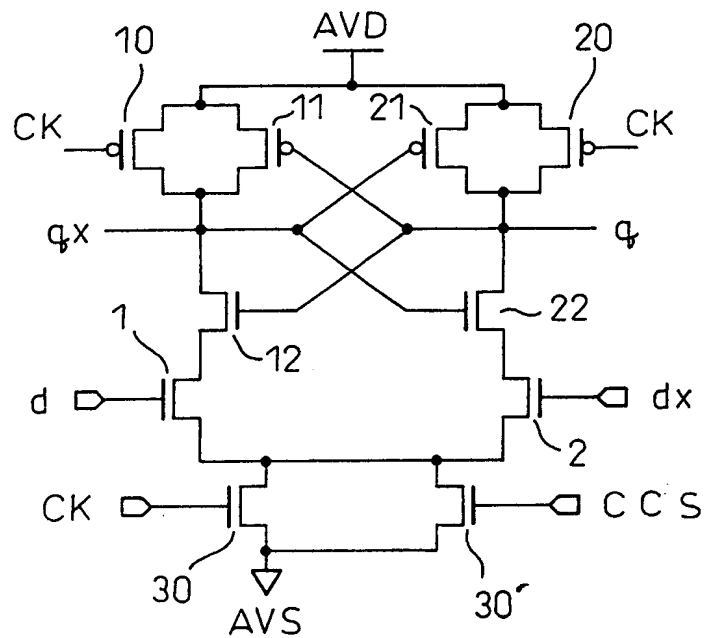
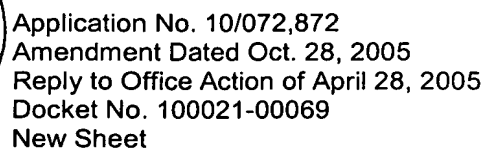




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Fig.26

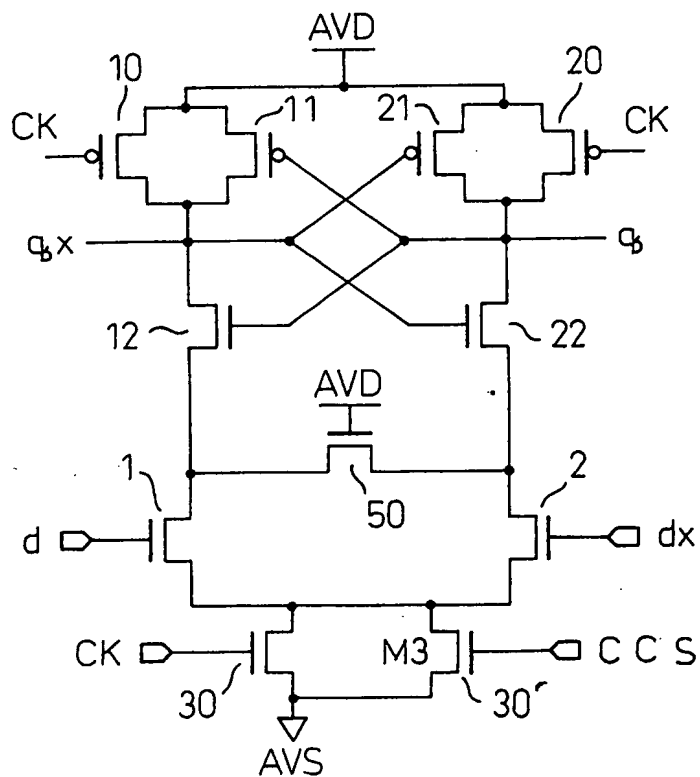






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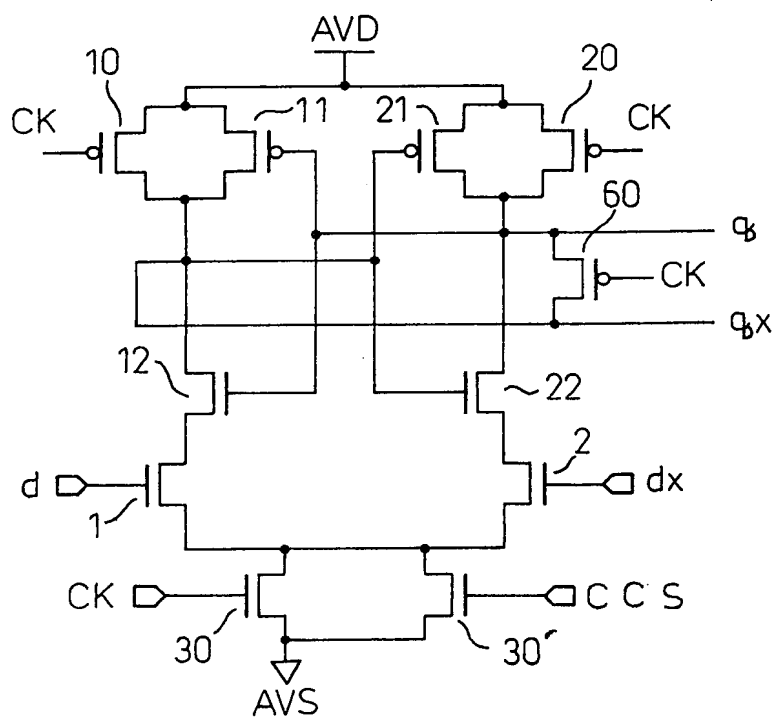
Fig. 28

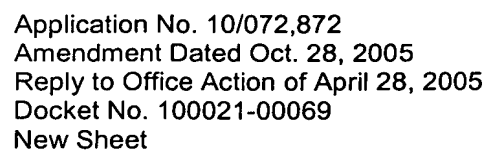


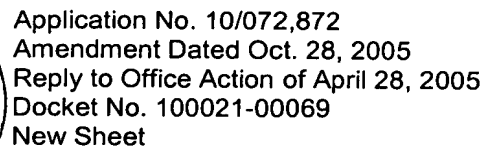


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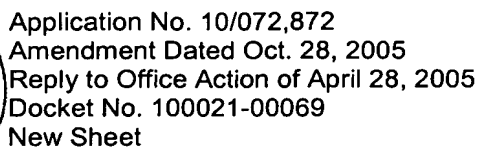
Fig. 29







The circuit diagram shows a differential amplifier stage followed by a differential-to-single-ended converter. The differential amplifier consists of a PMOS differential pair (10, 20) with gates connected to a common-mode feedback (CMFB) network (11, 21) and drains connected to a PMOS current mirror (60). The CMFB network is controlled by a clock signal CK. The differential pair is biased by an NMOS differential pair (1, 2) with gates connected to a common-mode feedback network (12, 22) and drains connected to an NMOS current mirror (50). The common-mode feedback network is also controlled by CK. The differential output of the NMOS pair is converted to a single-ended output (dx) by a PMOS current mirror (30, 30'). The gates of the NMOS pair are connected to a clock signal CK, and the gates of the PMOS pair are connected to a clock signal CK. The circuit is biased by a differential-mode feedback (DMFB) signal (AVD) and a common-mode feedback (CMFB) signal (AVS).

[illegible]